WHAT IS CLAIMED IS:

1. A method for transmitting data among processors over a plurality of parallel data lines and a clock signal line, the method comprising:

receiving at a receiver processor data transmitted from a sender processor;

receiving at said receiver processor a clock signal transmitted from said sender processor;

phase aligning at said receiver processor a bit of said data with said clock signal, said phase aligning comprising:

selecting a data phase from a plurality of data phases in a delay chain;

checking for a round-off error in said selecting a data phase and setting a round-off error flag if said round-off error is present; and

adjusting said selected data phase to compensate for said round-off error if said round- off error flag is set.

2. The method of claim 1 wherein said selecting a data phase from a plurality of data phases in a delay chain includes:

locating a late guard band inverter address in the delay chain that corresponds to a leading edge of said bit of said data;

locating an early guard band inverter address in the delay chain that corresponds to a trailing edge of said bit of said data;

calculating a midpoint inverter address in the delay chain by adding said late guard band inverter address to said early guard band inverter address and then dividing by two; and

outputting said selected data phase, said selected data phase corresponding to said midpoint inverter address.

3. The method of claim 2 wherein said checking for a round-off error includes:

isolating a least significant bit of sum of said late guard band inverter address and said early guard band inverter address; and

setting said round-off error flag if said least significant bit is an odd number.

4. The method of claim 1 wherein said adjusting said selected data phase includes:

sending said selected data phase into a half-delay; and

outputting said adjusted data phase, said data adjusted data phase corresponding to output of said half-delay.

5. The method of claim 1 wherein said adjusting said selected data phase includes:

responding to a cycle delay signal.

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6. A system for transmitting data among processors over a plurality of parallel data lines and a clock signal line, the system comprising:

a processor with the circuitry and logic to perform the method comprising:

receiving at a receiver processor data transmitted from a sender processor;

receiving at said receiver processor a clock signal transmitted from said sender processor;

phase aligning at said receiver processor a bit of said data with said clock signal, said phase aligning comprising:

selecting a data phase from a plurality of data phases in a delay chain;

checking for a round-off error in said selecting a data phase and setting a round-off error flag if said round-off error is present; and

adjusting said selected data phase to compensate for said round-off error if said round- off error flag is set.

7. The system of claim 6 wherein said selecting a data phase from a plurality of data phases in a delay chain includes:

locating a late guard band inverter address in the delay chain that corresponds to a leading edge of said bit of said data;

locating an early guard band inverter address in the delay chain that corresponds to a trailing edge of said bit of said data;

calculating a midpoint inverter address in the delay chain by adding said late guard band inverter address to said early guard band inverter address and then dividing by two; and

outputting said selected data phase, said selected data phase corresponding to said midpoint inverter address.

8. The system of claim 7 wherein said checking for a round-off error includes:

isolating a least significant bit of sum of said late guard band inverter address and said early guard band inverter address; and

setting said round-off error flag if said least significant bit is an odd number.

9. The system of claim 6 wherein said adjusting said selected data phase includes:

sending said selected data phase into a half-delay; and

outputting said adjusted data phase, said data adjusted data phase corresponding to output of said half-delay.

10. The system of claim 6 wherein said adjusting said selected data phase includes: responding to a cycle delay signal.

11. A storage medium encoded with machine-readable computer program code for transmitting data among processors over a plurality of parallel data lines and a clock signal line, the storage medium storing instructions for causing a computer system to implement a method comprising:

receiving at a receiver processor data transmitted from a sender processor;

receiving at said receiver processor a clock signal transmitted from said sender processor;

phase aligning at said receiver processor a bit of said data with said clock signal, said phase aligning comprising:

selecting a data phase from a plurality of data phases in a delay chain;

checking for a round-off error in said selecting a data phase and setting a round-off error flag if said round-off error is present; and

adjusting said selected data phase to compensate for said round-off error if said round- off error flag is set.

12. The storage medium of claim 11 wherein said selecting a data phase from a plurality of data phases in a delay chain includes:

locating a late guard band inverter address in the delay chain that corresponds to a leading edge of said bit of said data;

locating an early guard band inverter address in the delay chain that corresponds to a trailing edge of said bit of said data;

calculating a midpoint inverter address in the delay chain by adding said late guard band inverter address to said early guard band inverter address and then dividing by two; and

outputting said selected data phase, said selected data phase corresponding to said midpoint inverter address.

13. The storage medium of claim 12 wherein said checking for a round-off error includes:

isolating a least significant bit of sum of said late guard band inverter address and said early guard band inverter address; and

setting said round-off error flag if said least significant bit is an odd number.

14. The storage medium of claim 11 wherein said adjusting said selected data phase includes:

sending said selected data phase into a half-delay; and

outputting said adjusted data phase, said data adjusted data phase corresponding to output of said half-delay.

15. The storage medium of claim 11 wherein said adjusting said selected data phase includes:

responding to a cycle delay signal.